In the Claims:

1. (Currently Amended) A method, comprising:

asserting an edge-triggered interrupt signal from an input/output interrupt controller to a local interrupt controller within a processor; and

delivering an interrupt pending signal from the processor to a power management device.

2. (Original) The method of claim 1, further comprising the power management device causing the processor to enter a high power state if the processor is in a low power state when the processor delivers the interrupt pending signal to the power management device.

3. (Original) The method of claim 2, wherein delivering an interrupt pending signal includes delivering the interrupt pending signal from the processor to the power management device over a single signal line coupled between a single processor pin and the power management device.

4. (Original) The method of claim 3, wherein causing the processor to enter a high power state includes the power management device deasserting a stop clock signal.

5. (Currently Amended) A method, comprising:

asserting an edge-triggered interrupt signal from an input/output interrupt controller to a local interrupt controller within a processor;

setting a bit within the processor indicating that an interrupt is pending; and

polling the processor to determine if an interrupt is pending.

6. (Original) The method of claim 5, wherein polling the processor to determine if an interrupt is pending includes polling the processor to determine if an interrupt is pending only if the processor is in a low power state.

7. (Original) The method of claim 6, further comprising causing the processor to enter a high power state if the polling of the processor reveals that an interrupt is pending.

8. (Original) The method of claim 7, wherein causing the processor to enter a high power state includes deasserting a stop clock signal delivered from a power management device to the processor.

9. (Original) A system, comprising:

a processor including a local interrupt controller and an interrupt pending signal output;

an input/output interrupt controller coupled to the processor, the input/output interrupt controller to deliver an edge-triggered interrupt signal to the processor; and

a power management device including an interrupt pending signal input coupled to the interrupt pending signal output of the processor, the processor to assert the interrupt pending signal in response to the delivery of the edge-triggered interrupt signal.

10. (Original) The system of claim 9, wherein the processor further includes a stop clock signal input, the processor to cease executing instructions in response to an assertion of the stop clock signal by the power management device.

11. (Original) The system of claim 10, the power management device to cause the processor to enter a high power state if the processor is in a low power state when it asserts the interrupt pending signal.

12. (Original) The system of claim 11, wherein the power management device causes the processor to enter the high power state be deasserting the stop clock signal.

13. Cancelled

14. Cancelled

15. Cancelled

16. Cancelled